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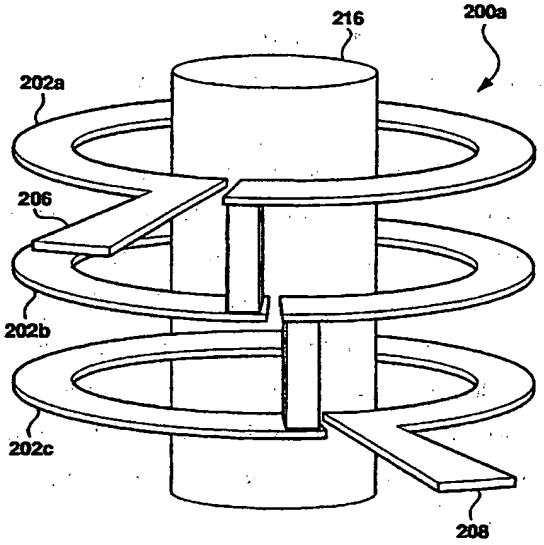
(54) Title: MULTI-LAYER INDUCTOR AND TRANSFORMER FORMED ON AN INTEGRATED CIRCUIT SUBSTRATE



(57) Abstract: An inductor (200) and transformer (402) comprise a plurality of interleaved conductive layers (202) and insulation layers fabricated on a monolithic semiconductor integrated circuit die. The conductive layers are shaped into coil turns of the inductor and the transformer, and are stacked vertically (perpendicular to the horizontal plane of the coil layers) and proximate to one another so as to achieve close magnetic coupling therebetween, thereby achieving a larger inductance value for a given sized coil structure. The conductive layer coil turns are connected together with conductive vias through the interposing insulation layers.

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MULTI-LAYER INDUCTOR AND TRANSFORMER FORMED ON AN INTERGRATED CIRCUIT SUBSTRATE

The present invention relates to passive components fabricated on a semiconductor integrated circuit die, and more particularly, to inductors and transformers fabricated on the integrated circuit die and comprising a plurality of conductive layers having insulation layers interleaved therebetween.

Analog electronic circuits, especially those operating at radio frequency, may include inductors and transformers for filtering, frequency mixing, oscillators, interstage radio frequency coupling, and high frequency pulse coupling. Transformers are adapted to pass alternating current (AC) signals and block direct current (DC). Inductors and transformers have been fabricated in many forms, from large iron core transformers used at power frequencies to air core inductors used at radio frequencies. Radio frequency inductors and transformers have been enclosed in metal cans, non-conductive coil forms, open construction, fabricated onto a printed circuit board and the like. More recently with the advent of integrated circuits and electronic miniaturization the need arose to reduce the size of external discrete components necessary with an integrated circuit product, preferably, elimination of any discrete components was a primary goal. More and more formerly discrete components were fabricated onto integrated circuits, i.e., resistors, capacitors and inductors, for both size and cost reasons. Inductors were especially a problem because of the physical size and geometry normally required for an effective inductor over a desired range of frequencies.

An inductor fabricated on an integrated circuit substrate generally has been formed in the shape of a spiral coil structure in a single metal layer on an insulation layer using typical integrated circuit fabrication techniques. This spiral coil structure requires a substantial area of the silicon integrated circuit substrate, typically for example, 200 μm x 200 μm. The spiral coil structure also suffers from parasitic capacitive influence from the integrated circuit substrate on which it is fabricated. Fabrication on an integrated circuit substrate of an efficient transformer (two inductors electromagnetically coupled together) is also extremely difficult using spiral coil structure shapes because of the physical size required and the inherent parasitic capacitance which may render the resulting transformer structure inefficient or ineffective for a desired purpose.

What is needed are more effective and efficient inductor and transformer structures that may be easily and inexpensively fabricated on an integrated circuit substrate and do not have to occupy a substantial area of the substrate.

The present invention overcomes the above-identified problems as well as other shortcomings and deficiencies of existing technologies by providing on a monolithic semiconductor integrated circuit die an inductor comprising a plurality of conductive layers shaped into coil turns and interleaved with a plurality of insulation layers. The conductive layer coil turns are stacked vertically (perpendicular to the horizontal plane of the conductive coil layers) and proximate to one another so as to achieve close magnetic coupling therebetween, thereby achieving a larger inductance value for a given sized coil structure. The conductive layer coil turns are connected together with conductive vias through the interposing insulation layers. It is contemplated and within the scope of the present invention that the conductive layer coil turns may be of any shape, such as for example but not limitation, round, square, triangular, oval, hexagonal and the like.

According to an embodiment of the invention, a transformer may be fabricated in a similar fashion by having concentric or co-axial inductors formed from the plurality of conductive coil layers with a plurality of

insulation layers interleaved therebetween. The vertically stacked conductive coil layers of each of the individual inductors of the transformer are connected together with conductive vias through the interposing insulation layers. The conductive vias may include a plurality of vias connecting adjacent conductive coil layers so as to keep series resistance low in the connection thereof. The conductive layers (coil turns) andvias may be made from metal such as copper, aluminum, alloys and the like; doped polysilicon, or any other type of conductive material that may be used in the fabrication of circuits and connections on an integrated circuit substrate.

In an embodiment of the present invention, fabricated on a monolithic semiconductor integrated circuit die is a plurality of conductive layers with a plurality of insulation layers therebetween. The conductive and insulation layers are interleaved one with the other. Each of the plurality of coil turn conductive layers has substantially the same diameter and an insulation layer is interposed between two adjacent coil turn conductive layers. The insulation layer is only as thick as required, resulting in the adjacent coil turn conductive layers having increased magnetic coupling and reduced parasitic capacitance with the substrate. In addition, the adjacent closely spaced and vertically stacked coil turns have substantially the same voltage potential thereon so that capacitive coupling therebetween is minimized. Only one coil turn is adjacent to the integrated circuit substrate and has a relatively small footprint. This greatly reduces parasitic capacitance from the substrate. Conductive Vias are formed in the insulation layers between adjacent coil turns of the conductive layers and connect the end points (open portions) of the adjacent coil turns together.

In another embodiment of the present invention, the plurality of conductive layers having a plurality of insulation layers therebetween are arranged as two inductor coils. The two coils are concentric, one of the inductor coils located within the other one and coaxially aligned therein. Each conductive layer comprises a coil turn for each of the two inductor coils. The conductive and insulation layers are interleaved one with the other. The one (first) of the two inductor coils has a larger inside diameter then the outside diameter of the other one (second) of the two coils, wherein the second inductor coil fits inside of the first inductor coil and is concentric therewith. It is contemplated and within the scope of the present invention that the first and second inductor coils have the same number of turns (same number of layers) or a different number of turns (some of the conductive layers not used by one or the other of the two inductor coils). Thus impedance matching and/or voltage step-up or step-down between the input and output of the transformer may be readily achieved with this embodiment of the invention. The adjacent coil turn conductive layers have increased magnetic coupling therebetween and reduced parasitic capacitance with the substrate. In addition, the adjacent closely spaced and vertically stacked coil turns have substantially the same voltage potential thereon so that capacitive coupling therebetween is minimized. Only one coil turn of each of the two inductor coils is adjacent to the integrated circuit substrate and has a relatively small footprint. This greatly reduces parasitic capacitance from the substrate to the transformer. Conductive Vias are formed in the insulation layers between adjacent coil turns of the conductive layers and connect the end points (open portions) of the adjacent coil turns together.

According to the aforementioned embodiments of the present invention, the insulation layers between the coil turns of the inductor(s) may preferably be very thin so that the adjacent turns of the coil are close together, thus, improving the magnetic coupling therebetween and increasing the effective inductance for a given size coil diameter. It is also contemplated and within the scope of the present invention that a material of high magnetic permeability may be used by locating same within the coil so as to further increase the effective

inductance value for a give size of coil structure. This material may be, for example but not limitation: iron, iron oxide, ferrite ceramic, ferrous oxide or other materials that increase the effective inductance value of the inductor coil and transformer.

An advantage of the present invention is that the inductor/transformer structure occupies less area of the integrated circuit substrate.

Another advantage is that parasitic capacitance of the integrated circuit substrate is reduced.

Still another advantage is mutual inductance or inductive coupling between the two coils of the transformer is enhance because of the close proximity of the two coils.

A feature of the present invention is fabricating a coil inductor on a semiconductor integrated circuit die by depositing each conductive layer turn of the coil on a respective insulation layer and connecting the turns together with conductive vias through these respective insulation layers.

Yet another feature is using a plurality of vias between adjacent conductive layer turns to reduce the connection resistance therebetween.

Another feature is positioning a second coil concentrically inside of a first coil on an integrated circuit substrate so that both of the first and second coils are in coaxial alignment and electromagnetically coupled together to form a transformer.

Still another feature is impedance matching with a transformer fabricated on the integrated circuit substrate.

Another feature is placing a magnetic material within the coil fabricated on the integrated circuit substrate for increasing the inductance thereof.

Yet another feature is AC voltage step-up and step-down with a transformer fabricated on the integrated circuit substrate.

Other and further features and advantages will be apparent from the following description of presently preferred embodiments of the invention, given for the purpose of disclosure and taken in conjunction with the accompanying drawings.

Figure 1 is a schematic plan view of a prior art inductor comprising a spiral wound coil fabricated on an integrated circuit substrate;

Figure 2 and is a schematic diagram of inductors, according to embodiments of the present invention;

Figure 2A is a schematic diagram of transformers, according to embodiments of the present invention;

Figure 3 is a schematic orthogonal view of a coil portion of the embodiment of the invention illustrated in Figure 2;

Figure 3A is a schematic orthogonal view of a coil portion having a magnetic core of the embodiment of the invention illustrated in Figure 2;

Figure 4 is a schematic plan view of a transformer portion of the embodiment of the invention illustrated in Figure 2A;

Figure 4A is a schematic plan view of a transformer portion having a magnetic core of the embodiment of the invention illustrated in Figure 2A; and

Figure 5 is a schematic elevational cross-section view of the inductor coil structure of Figure 3, fabricated on a semiconductor integrated circuit die.

Referring to Figure 1, a schematic diagram of a prior art inductor comprising a spiral wound coil fabricated on an integrated circuit substrate is illustrated. The spirally wound coil 102, having a first end 104 and a second end 106, is interposed on an insulation layer (not illustrated) of a semiconductor integrated circuit substrate 108. The flat spiral wound coil 102 suffers from parasiticcapacitive coupling to the substrate 108, and requires a great deal of area on the substrate 102.

The present invention is an inductor, fabricated on monolithic semiconductor integrated circuit die, comprising a plurality of conductive layers shaped into coil turns and interleaved with a plurality of insulation layers. It is contemplated and within the scope of the present invention that a plurality of inductors may be a fabricated as disclosed herein, and that the plurality of inductors may be positioned in relation to one another for electromagnetic coupling therebetween to form a transformer. It is also contemplated and within the scope of the present invention that the conductive layer coil turns may be of any shape, such as for example but not limitation, round, square, triangular, oval, hexagonal and the like.

Referring now to the drawings, the details of preferred embodiments of the present invention are schematically illustrated. Like elements in the drawings will be represented by like numbers, and similar elements will be represented by like numbers with a different lower case letter suffix.

Referring to Figure 2, a schematic diagram of inductors of the embodiments of the invention is illustrated. An inductor of the present invention is generally represented by the numeral 200, and another inductor of the present invention having a magnetic core 216 proximate to the coil turns is generally represented by the numeral 200a. The inductors 200 and 200a have a first node 206 and an second node 208.

Referring to Figure 2A, a schematic diagram of the inductors arranged as a transformer of the embodiments of the invention is illustrated. A transformer of the present invention is generally represented by the numeral 210, and another transformer of the present invention having a magnetic core 216 is generally represented by the numeral 210a. A first coil 212 and a second coil 214 comprise the transformer 210. The transformer 210 has input nodes 218, 218a for the coil 212, and output nodes 220 and 220a for the coil 214. One of ordinary skill in the art will readily understand that the input nodes 218 and the output nodes 220 may be reversed or switched for inverting the phase of the input signal by 180 degrees at the output. Also the coils 212 and 214 may be interchanged as output and input coils, respectively. In addition, the number of coil turns (conductive layers used) may be different for the coil 212 and the coil 214, thereby obtaining an impedance change or voltage step-up or step-down depending on the turns ratio of coil 212 and coil 214.

Referring now to Figure 3, a schematic orthogonal view of a coil portion of the inductor 200 is illustrated. The inductor 200 is fabricated on a semiconductor integrated circuit substrate (not illustrated). The inductor 200 is comprised of a plurality of turns formed from conductive layers that are coil shaped. These coil shaped conductive layers, illustrated in Figure 3 as coil turns 202a, 202b and 202c, are formed on a plurality of insulation layers (not illustrated for clarity). Each coil shaped conductive layer is formed on a respective insulation layer (See Figure 5). Conductive Vias are formed in the insulation layers between adjacent coil turns of the conductive layers and connect the end points (open portions) of the adjacent coil turns together (See Figure 5). The conductive layers (coil turns) andvias may be made from metal such as copper, aluminum, metal alloys and the like; doped polysilicon, or any other type of conductive material that may be used in the fabrication of circuits and connections on an integrated circuit substrate.

Referring to Figure 3A, a schematic orthogonal view of the coil portion of the inductor 200a having a magnetic core 216 to increase the inductance of the coil 200a is illustrated. The magnetic core 216 is comprised of a material of high magnetic permeability and is located, preferably, within the coil 200a so as to further increase the effective inductance for a give size of coil structure. This material may be, for example but not limitation, iron oxide, ferrite ceramic, ferrous oxide or other materials that increase the effective inductance of the inductor coil.

Referring to Figure 4, a schematic plan view of a transformer portion of the embodiment of the invention in Figure 2A is illustrated. The first coil 212 has the input 218 and a via 404 which connects the illustrated conductive layer coil turn end point of the first coil 212 to the end point of the next adjacent coil turn thereof (see Figure 5). In the same fashion, the second coil 214 has the input 220 and a via 406 which connects the illustrated conductive layer coil turn end point of the second coil 214 to the end point of the next adjacent coil turn (see Figure 5). The first and second coils 212 and 214 are concentric, in coaxial alignment and close proximity. This enhances the mutual electromagnetic coupling therebetween. In addition, these adjacent, closely spaced and vertically stacked coil turns have substantially the same voltage potential thereon so thatcapacitive coupling therebetween is minimized.

Referring to Figure 4A, a schematic plan view of a transformer portion having a magnetic core to increase the inductance of the transformer is illustrated. The magnetic core 216 is comprised of a material of high magnetic permeability, and is, preferably, located within the coils 212 and 214 so as to further increase the effective inductance for a give size of coil structure of the transformer. This material may be, for example but not limitation, iron oxide, ferrite ceramic, ferrous oxide or other materials that increase the effective inductance of the inductor coil.

Referring now to Figure 5, a schematicelevational cross-section view of the conductive layer coil turns of the inductor 200 fabricated on a semiconductor integrated circuit substrate 510 is illustrated. A first coil turn 202d is formed over an insulation layer 516d. An end of the first coil turn 202d is connected to a connection node 208. An insulation layer 514c is formed over the first coil turn 202d. A second coil turn 202c is formed over the insulation layer 516c. Another insulation layer 516b is formed over the second coil turn 202c. A third coil turn 202b is formed over the insulation layer 516b. Still another insulation layer 516a is formed over the third coil turn 202b. Yet another insulation layer 514a is formed over the third coil turn 202b. A fourth coil turn 202a is formed over the insulation layer 516a. Another insulation layer 518 may be formed over the fourth coil turn 202a. An end of the fourth coil turn 202d is connected to the connection node 206. Vias (represented by the vertical conductive connections in Figure 5) interconnect the end portions of the coil turns 202a and 202b, 202b and 202c, and 202c and 202d, respectively. It is contemplated and with the scope of the present invention that any number of coil turns and insulation layers may used.

The present invention, therefore, is well adapted to carry out the objects and attain the ends and advantages mentioned, as well as others inherent therein. While the present invention has been depicted, described, and is defined by reference to particular preferred embodiments of the invention, such references do not imply a limitation on the invention, and no such limitation is to be inferred. The invention is capable of considerable modification, alternation, and equivalents in form and function, as will occur to those ordinarily skilled in the pertinent arts. The depicted and described preferred embodiments of the invention are exemplary only, and are

not exhaustive of the scope of the invention. Consequently, the invention is intended to be limited only by the spirit and scope of the appended claims, giving full cognizance to equivalents in all respects.

CLAIMS

1. An integrated circuit apparatus having an inductor thereon, said apparatus comprising:

an integrated circuit substrate;

a first insulation layer over a face of said integrated circuit substrate;

a plurality of conductive layers, each of said plurality of conductive layers in the shape of a coil turn, the coil turn having a first and a second end;

a plurality of insulation layers interleaved between said plurality of conductive layers;

a one of said plurality of conductive layers proximate to said first insulation layer and the other ones of said plurality of conductive layers stacked over the one with said plurality of insulation layers interleaved therebetween; and

a plurality of conductive vias connecting adjacent ones of the coil turns of said plurality of conductive layers, thereby forming an inductor coil.

2. The apparatus of claim 1, wherein respective ones of said plurality of conductivevias connect the second ends of each one of the coil turns of said plurality of conductive layers to the first ends of each of the adjacent ones of the coil turns of said plurality of conductive layers, thereby forming the inductor coil.

3. The apparatus of claim 1, further comprising a magnetic material interposed concentrically inside of an inner diameter of the coil turns of said plurality of conductive layers so as to increase the inductance thereof.

4. An integrated circuit apparatus having a transformer thereon, said apparatus comprising:

an integrated circuit substrate;

a first insulation layer over a face of said integrated circuit substrate;

a plurality of conductive layers, each of said plurality of conductive layers shaped in the form of a first coil turn and a second coil turn wherein the first coil turn is concentrically located within the second coil turn, the first and second coil turns each having first and second ends;

a plurality of insulation layers interleaved between said plurality of conductive layers;

a one of said plurality of conductive layers proximate to said first insulation layer and the other ones of said plurality of conductive layers stacked over the one with said plurality of insulation layers interleaved therebetween; and

a plurality of conductive vias connecting adjacent ones of the first and second coil turns of said plurality of conductive layers, thereby forming a transformer comprising a first coil and a second coil.

5. The apparatus of claim 4, wherein respective ones of said plurality of conductive viasconnect second ends of each of the ones of the first and second coil turns of said plurality of conductive layers to first ends of each of the adjacent ones of the first and second coil turns, respectively, of said plurality of conductive layers, thereby forming the first and second coils which are concentrically aligned.

6. The apparatus of claim 4, further comprising a magnetic material interposed inside of an inner diameter of the first coil turn of said plurality of conductive layers so as to increase the inductance thereof.

7. The apparatus of claim 4, wherein the number of the first coil turns connected together to form the first coil is different then the number of the second coil turns connected together to form the second coil, wherein an impedance change occurs between the first and second coils.

8. The apparatus of claim 4, wherein the number of the first coil turns connected together to form the first coil is different then the number of the second coil turns connected together to form the second coil, wherein a voltage change occurs between the first and second coils.

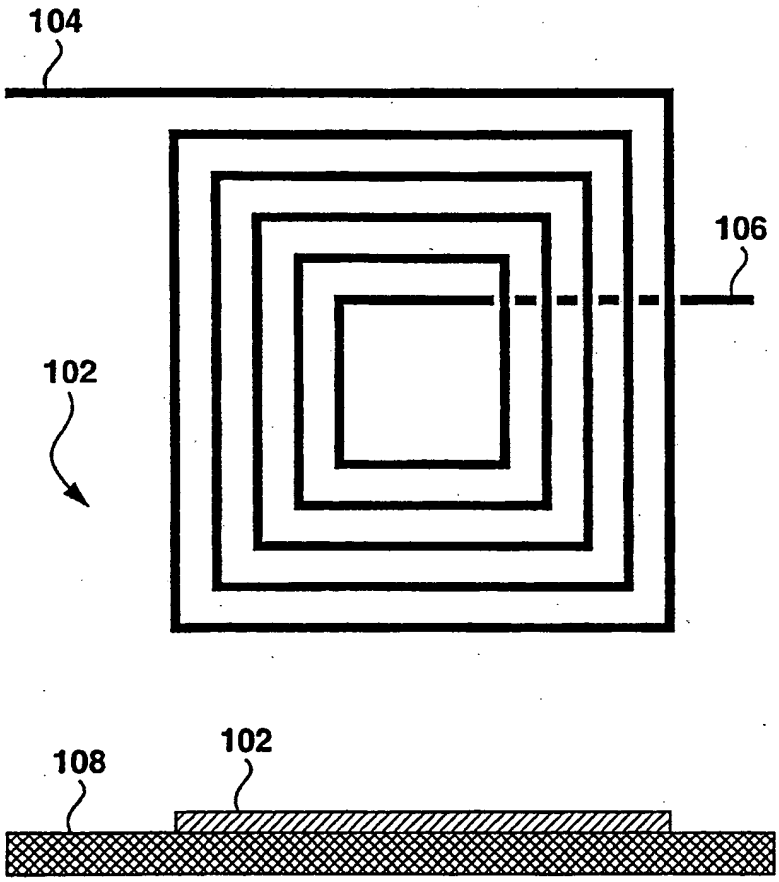
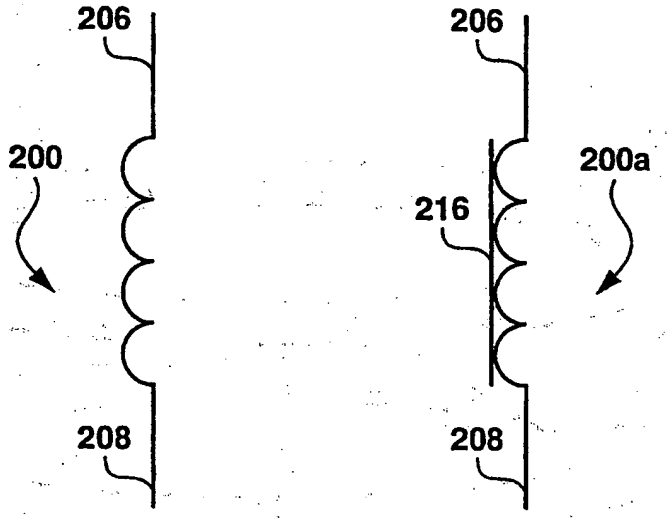


Fig. 1 (PRIOR ART)


206
200
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206
216
200a
208

Fig. 2

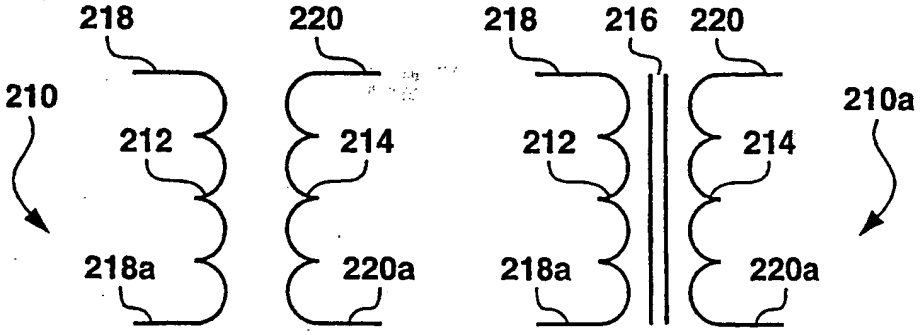
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Fig. 2A

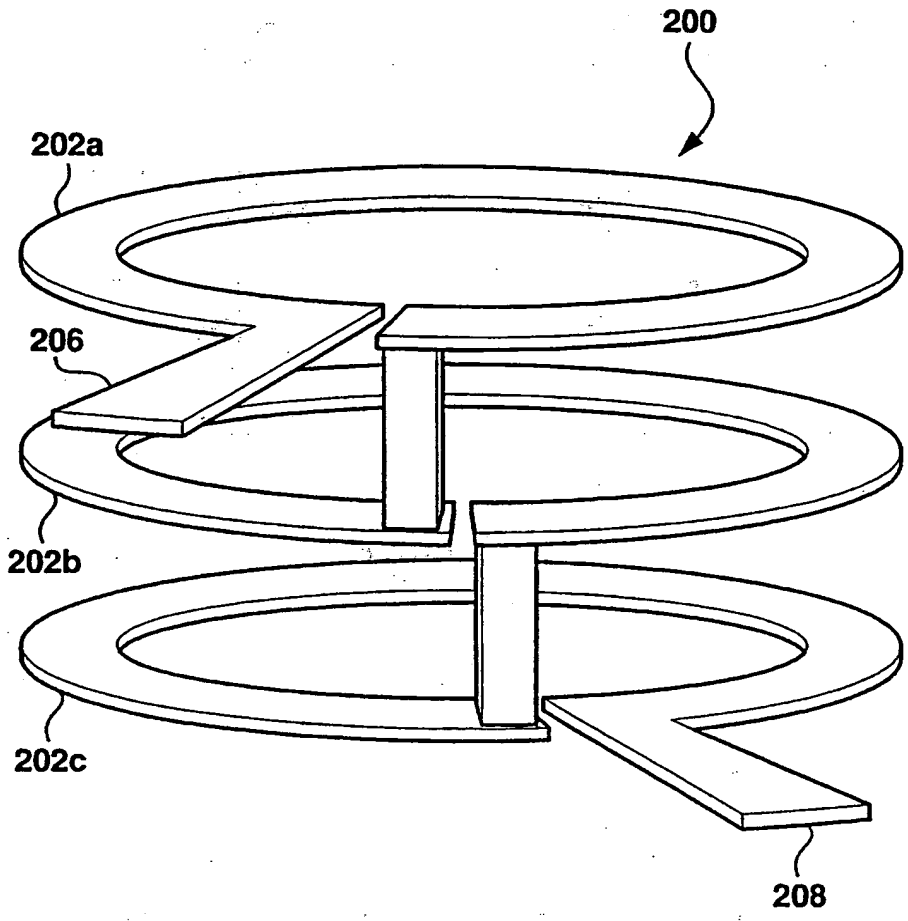

Fig. 3

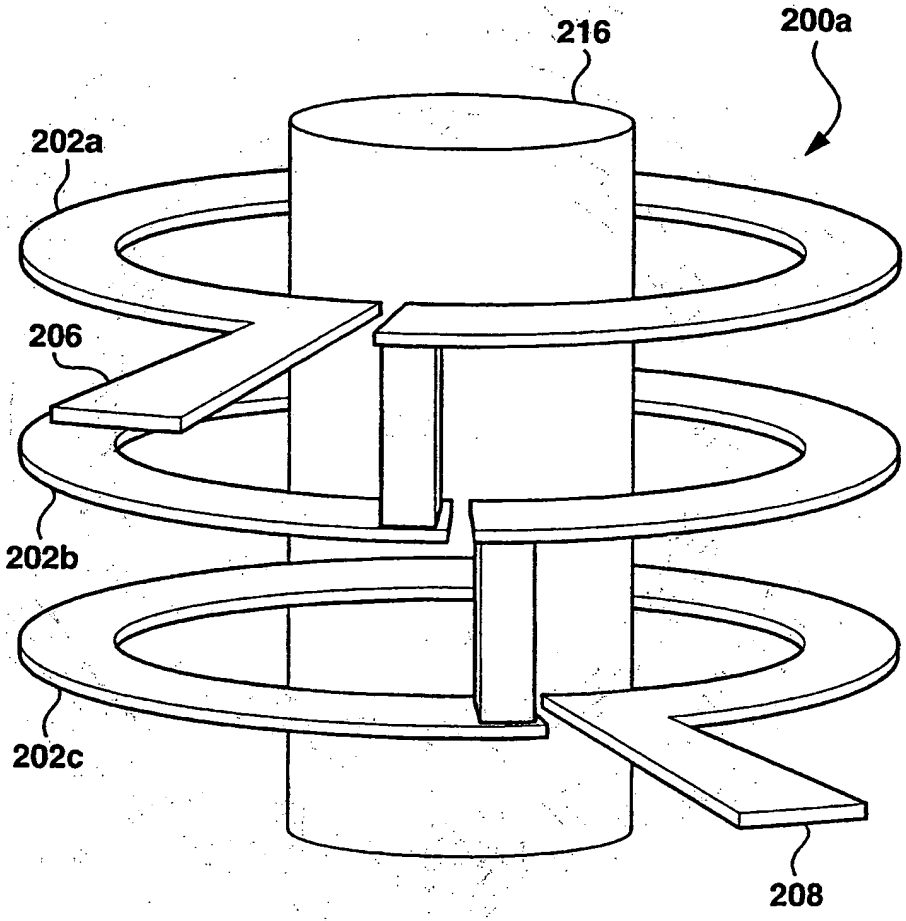

Fig. 3A

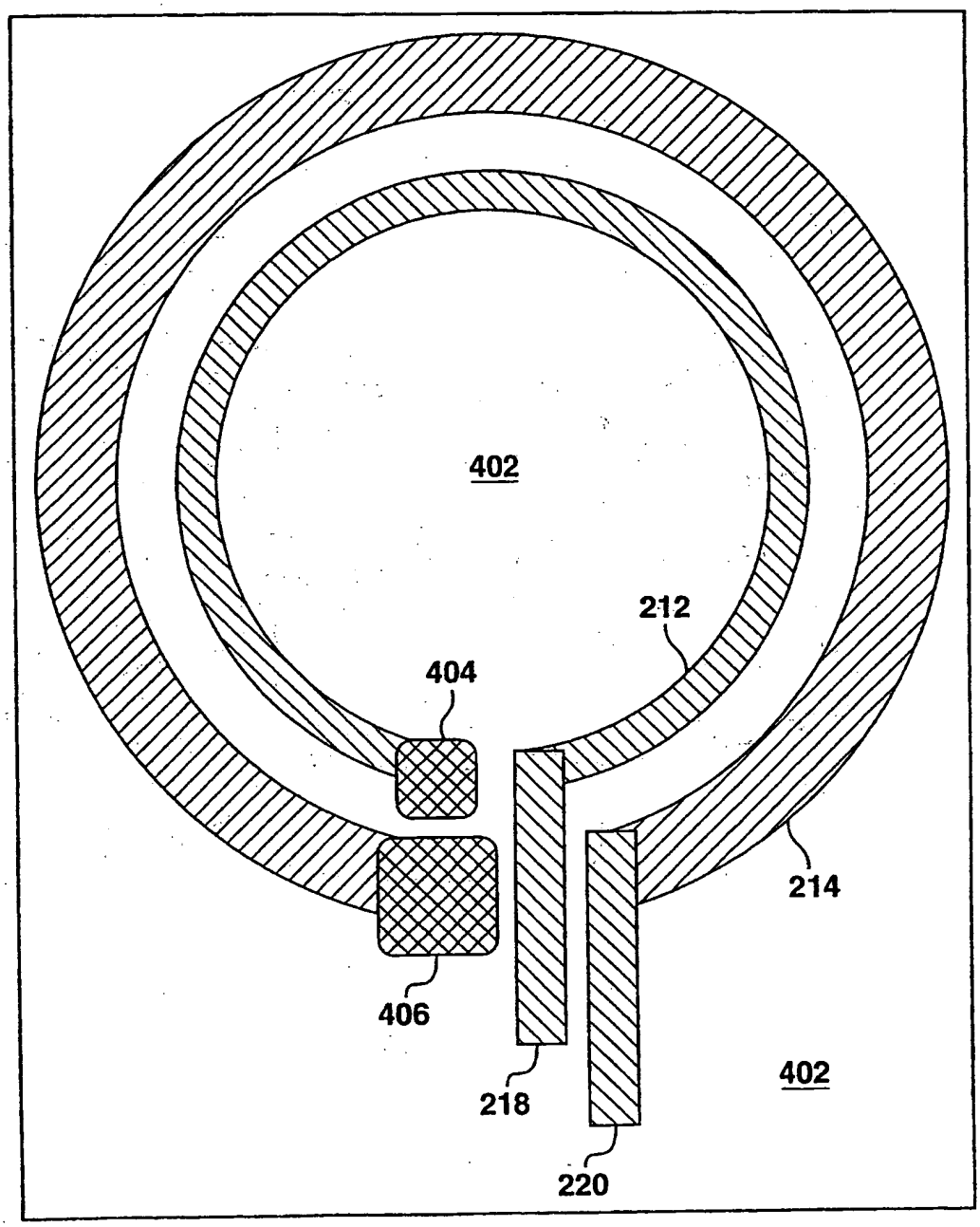

Fig. 4

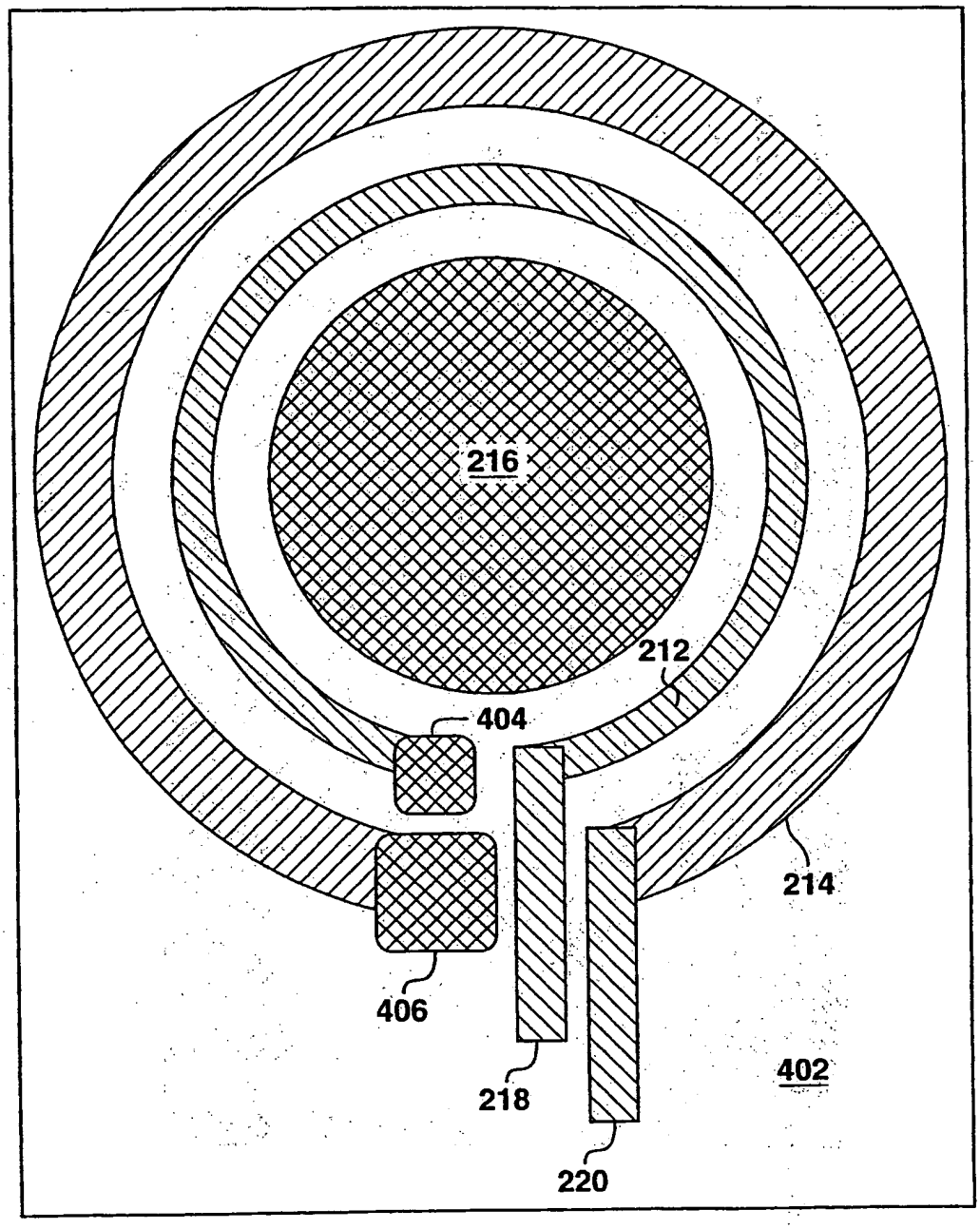

Fig. 4A

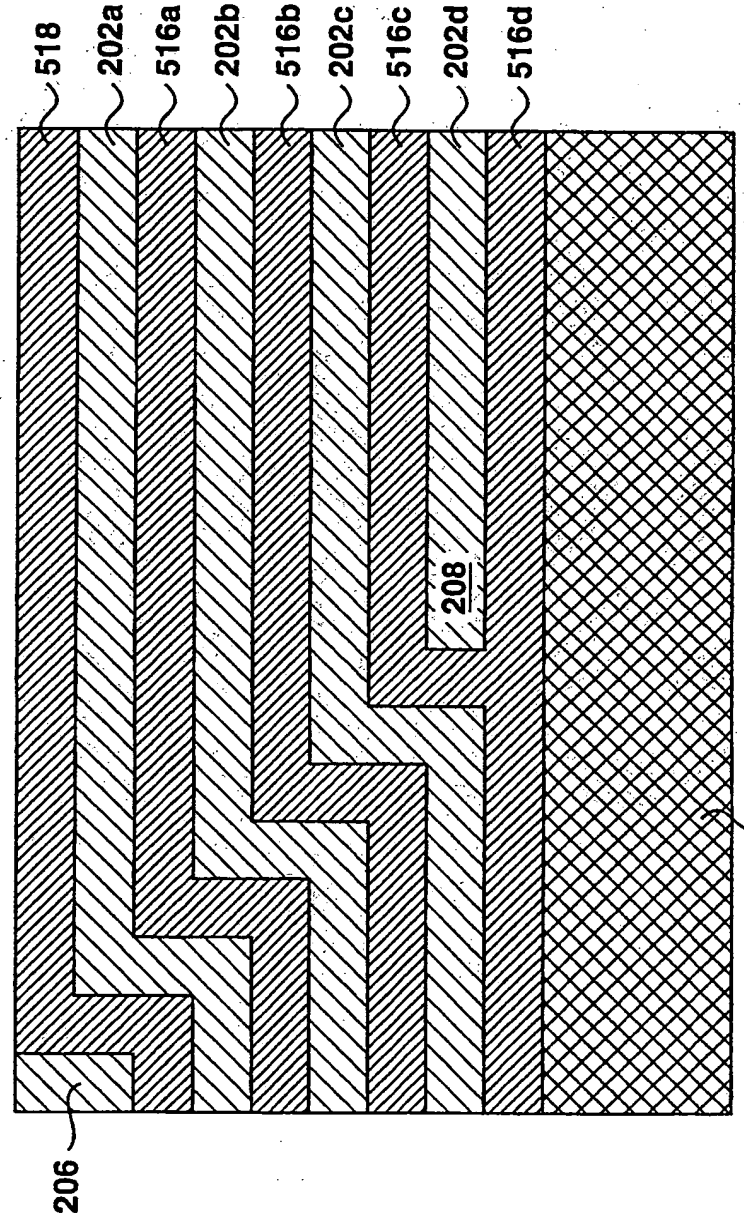

Fig. 5

INTERNATIONAL SEARCH REPORT

Interr ıal Application No
PCT/US 00/24412

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H01F17/00 H01L23/64

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H01F H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, PAJ

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
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X Y	PATENT ABSTRACTS OF JAPAN vol. 018, no. 290 (E-1557), 2 June 1994 (1994-06-02) -& JP 06 061058 A (ROHM CO LTD), 4 March 1994 (1994-03-04) abstract	1,2 3
X Y	US 3 785 046 A (JENNINGS T) 15 January 1974 (1974-01-15) column 4, line 35 -column 6, line 41; figure 15	4,5 6
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[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

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"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

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"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
29 November 2000	12/12/2000

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Edmeades, M

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INTERNATIONAL SEARCH REPORT

Interr ial Application No
PCT/US 00/24412

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

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